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EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,281	TAGGART ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6-17 and 19-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17 and 19-27* is/are allowed.

6)☒ Claim(s) *1,2,6-16 and 28-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ :
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 2 is rejected under 35 U.S.C. 102(e) as being anticipated by US 6,489,682 B1 (Yeh).

Yeh discloses, referring primarily to figures 1 and 2, an article comprising: a wire-bonding mounting substrate (102) including an upper protective layer (upper dielectric, shown not specifically referenced), a lower protective layer (bottom dielectric, shown not specifically referenced); a first wire-bond pad (104); and a first via (shown not referenced) in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, and wherein the first via is disposed directly below the first wire-bond pad, wherein the wire-bonding mounting substrate includes a first edge, the article further including: a second wire-bond pad (103); a second via (103v) in the wire-bonding mounting substrate, wherein the second via is in electrical contact with the second wire-bond pad, and wherein the second via is disposed directly below the

second wire-bond pad; and wherein the first via and the second via are staggered with respect to the first edge of the wire-bonding mounting substrate (figure 1) [claim 2].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 6-12, and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,489,682 B1 (Yeh) in view of US 6,252,178 B1 (Hashemi).

Yeh discloses, referring primarily to figure 1, an article comprising: a wire-bonding mounting substrate (102) including an upper protective layer (upper dielectric, shown not specifically referenced), a lower protective layer (bottom dielectric, shown not specifically referenced); a first wire-bond pad (104); and a first via (shown not referenced) in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, wherein the first via includes a liner that is electrically conductive, wherein the first via penetrates the upper protective layer and the lower protective layer (figure 1) and wherein the first via is disposed symmetrically and directly below the first wire-bond pad. Yeh does not specifically teach wherein the via includes an interconnect filling the via [claim 1]. However, Hashemi teaches a via including a liner (col. 3, lines 60-66), further including; an interconnect (260) filling the via. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to include an interconnect filling the via of Yeh. The motivation for doing so would have been to provide an anchor for the conductive pads on the opposite sides of the via.

Regarding claims 6 & 7, Yeh discloses the claimed invention as described above except Yeh does not specifically teach wherein the wire-bond pad includes a first layer and a second layer, wherein at least one of the first layer and the second layer is selected from a precious metal, a precious metal alloy, silver, gold, platinum, nickel, palladium, platinum, cobalt, rhodium, iridium, and combinations thereof [claim 6],

wherein the wire-bond pad includes a first layer and a second layer, and wherein the second layer is one of identical material to the first layer, or at least one of a more noble, or a softer metal than the first layer [claim 7]. However, Hashemi teaches a wire-bond pad including a first layer and a second layer, wherein at least one of the first layer and the second layer is selected from a precious metal, a precious metal alloy, silver, gold, platinum, nickel, palladium, platinum, cobalt, rhodium, iridium, and combinations thereof, wherein the wire-bond pad includes a first layer and a second layer, and wherein the second layer is one of identical material to the first layer, or at least one of a more noble, or a softer metal than the first layer. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to add a second layer of gold over the first layer of the wire bond pad in the modified invention of Yeh as taught by Hashemi. The motivation for doing so would have been to improve adhesion between the wire bond pad and the wire bond wire.

Similarly, Yeh discloses, referring primarily to figures 1-2, a package comprising: a wire-bonding mounting substrate (102) including an upper protective layer (upper dielectric, shown not specifically referenced), a lower protective layer (bottom dielectric, shown not specifically referenced); a first wire-bond pad (104); and a first via (shown not referenced) in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, wherein the first via includes a liner that is electrically conductive, wherein the first via penetrates the upper protective layer and the lower protective layer (figure 1), and wherein the first via is disposed symmetrically and directly below the first wire-bond pad; a die (101); and a first wire bond (107b) that

couples the die to the first wire-bond pad. Yeh does not specifically teach wherein the via includes an interconnect filling the via [claim 8]. However, Hashemi teaches a via including a liner (col. 3, lines 60-66), further including; an interconnect (260) filling the via. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to include an interconnect filling the via of Yeh. The motivation for doing so would have been to provide an anchor for the conductive pads on the opposite sides of the via. Additionally, the modified invention of Yeh teaches further including: a second wire-bond pad (103) disposed upon the first surface; a second via (103v) in the wire-bonding mounting substrate, wherein the second via is in electrical contact with the second wire-bond pad, and wherein the second via is disposed directly below the second wire-bond pad [claim 9], further including: a second wire-bond pad (103) disposed upon the first surface; a second via (103v) in the wire-bonding mounting substrate, wherein the second via is in electrical contact with the second wire-bond pad, and wherein the second via is disposed directly below the second wire-bond pad; a second bond wire (shown not specifically referenced) that couples the die to the second wire-bond pad; and wherein the respective lengths of the first bond wire and the second bond wire are adjusted so as to tune the package (col. 2, lines 1-10) [claim 10], further including: a first bump (shown not specifically referenced) coupled to the first via [claim 11], further including: a first bump (shown not specifically referenced) coupled to the first via; and a first trace (104p) that makes an electrical contact to the first bump [claim 12], wherein the first wire-bond pad is part of a plurality of wire-bond pads, and wherein each wire-bond pad is directly above a corresponding via from a plurality of vias (figure

1) [claim 14], wherein the first wire-bond pad is part of a plurality of wire-bond pads, wherein each wire-bond pad is directly above a corresponding via from a plurality of vias, and wherein each via is coupled to a bump (figure 1) [claim 15], wherein the first wire-bond pad is part of a plurality of wire-bond pads, wherein each wire-bond pad is directly above a corresponding via from a plurality of vias, wherein each via is coupled to a bump, and wherein each bump is directly below a corresponding via (figure 1) [claim 16].

Claims 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walton in view of Yeh.

Walton discloses, referring primarily to figures 11A-B, a computing system comprising: a semiconductor device (232) having a die and dynamic random-access memory (162) coupled to the die. Walton does not specifically disclose that the semiconductor device comprises a wire-bonding mounting substrate including a first surface and a second surface; a first wire-bond pad disposed upon the first surface; a first via in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, and wherein the first via is disposed symmetrically and directly below the first wire-bond pad; a die disposed on the first surface [claim 28]. Yeh discloses, a semiconductor device comprising: a wire-bonding mounting substrate (102) including an upper protective layer (shown not specifically referenced), a lower protective layer (shown not specifically referenced); a first wire-bond pad (104) disposed upon the first surface; a first via (shown not specifically referenced) in the wire-bonding

mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, wherein the first via includes a liner that is electrically conductive, wherein the first via penetrates the upper protective layer and the lower protective layer, and wherein the first via is disposed symmetrically and directly below the first wire-bond pad; and a die (101). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use the semiconductor device taught by Yeh as the semiconductor device in the invention of Walton. The motivation for doing so would have been to use a semiconductor device encapsulated from dust (Yeh, 1, lines 30-35). Moreover, the modified invention of Walton teaches, wherein the computing system is disposed in one of a computer, a wireless communicator, a hand-held device, an automobile, a locomotive, an aircraft, a watercraft, and a spacecraft (Walton – col. 4, lines 50-55) [claim 29], wherein the die is selected from a data storage device, a digital signal processor, a micro controller, an application specific integrated circuit, and a microprocessor (Walton – col. 5, lines 30-40) [claim 30].

Response to Arguments

Applicant's arguments filed 01 March 2007 have been fully considered but they are not persuasive.

Applicant's arguments with respect to claims 1, 3, 4, 8-12, and 14-16 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the Hashemi reference, Applicant argues, "To apply Hashiemi's structure to Yeh, would result in an impossibility as Hashemi has a core layer that prevents the filled via from penetrating a lower protective layer". However, Hashemi has

only been used to show that filling hollow vias with an interconnect material is known in the art. The invention of Yeh already discloses a hollow via which penetrates the upper and lower protective layers. The ordinarily skilled artisan would understand the desirability of filling the hollow with interconnect material as taught by Hashemi to increase the adhesion of the entire device.

Regarding claims 28-30, Applicant has not stated which limitations are supposedly lacking in the combination of Walton in view of Yeh. But as described above, the combination of Walton in view of Yeh and Hashemi does indeed teach the claimed inventions.

Regarding claim 2, Applicant has relied on the amendments to claim 1 for patenability. However, claim 2 does not included the amended limitations of claim 1, thus claim 2 stands on its own. Applicant has provided no separate arguments for claim 2.

Having addressed each of Applicants arguments, the traversal of the rejection on these grounds is deemed unsuccessful.

Allowable Subject Matter

Claims 17, and 19-27 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: Claim 17 states the limitation "wherein forming ceases upon contact with the first wire-bond pad". This limitation, in conjunction with the other claimed features, was neither found to be disclosed in, nor suggested by, the prior art. Claim 24 states the limitation "wherein forming ceases upon contact with the first wire-bond pad". This

limitation, in conjunction with the other claimed features, was neither found to be disclosed in, nor suggested by, the prior art.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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JCSN